A back-gate current neutralisation feedback loop for high input impedance neural front-end amplifiers

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A back-gate current neutralisation feedback loop for high input impedance neural front-end amplifiers

Zhijun Zhou and Paul Warr

The front-end amplifier for neural signal applications forms the critical element for signal detection and pre-processing, which determines not only the fidelity of the biosignal, but also impacts power consumption and detector size. A back-gate current neutralisation feedback technique is proposed to compensate for input leakage currents generated by low noise amplifiers alongside signal leakage into the input bias network when in integrated circuit form. Significantly, this topology ensures the front-end amplifier maintains a high input impedance across the wide range of manufacturing and operational variations seen in integrated circuits.

Introduction: Growing interest in the field of neuroscience leads to a rapid acceleration of the development of neural activity monitoring systems [1]. The Front-End Amplifier (FEA) is a key element for such systems. Neuroscientists and clinicians can simultaneously observe and record larger arrays of neural data, due to the integrated FEA providing a small die area. However, future multiple electrodes and multi-channel monitoring systems are restricted by a lack of suitable Integrated Circuit (IC) techniques.

The amplitude and frequency range commonly seen in electrically-observable neural signals are summarised in the introduction section of [2]. The impedance of the sensor-seen neural interface forms a voltage divider with respect to the FEA. A high input impedance FEA prevents signal attenuation in neural data acquisition. Furthermore, it minimises the current into the neuron to protect the tissue from damage, especially as multiple-channel systems become standard practice in neural sensing applications [2].

The input impedance of the FEA is reduced by the leakage current of the low-noise operational amplifier (OPAMP). It becomes the majority current in IC form after bias network bootstrapping and given the use pseudo resistors (PRs). PRs yield a large resistance within an acceptable die area, by connecting two Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) back-to-back to force the transistors into the subthreshold region [3].

The conventional neutralisation technique compensates the input leakage current of the OPAMP, via a capacitor [3]. It yields a real-time high input impedance for the FEA on an IC platform to avoid any external digital controllers, to reduce the circuit complexity and power consumption. However, it suffers from the need for a precise matching between the feedback capacitor and the input gate capacitance. For Complementary metal–oxide–semiconductors (CMOSs), the voltage variation between terminals (source, gate, drain and body), changes the effective gate capacitance. This will bring about mismatch between the leakage current and neutralisation current, which leads to the reduction of the input impedance of the FEA and instability of the feedback loop. Therefore, a conventional fixed-value capacitor neutralisation (FCN) loop is not sufficient in an IC implementation in practice.

Back-gate current neutralisation feedback: The circuit topology of the back-gate current neutralisation feedback (BCN) technique is depicted in Fig. 1. The OPAMPs A1 and A2 are low-noise two-stage CMOS amplifiers (shown in Fig. 2). The input signal, V_{in}, is connected to the '+' terminal of A1. The output of A1, V_{out}, is determined by the resistors,

$$V_{out} = \frac{R1 + R2}{R2} V_{in} \quad (1)$$

The resistors *R1* and *R2* are PRs to maximise resistance within small chip area. As shown in Fig. 1(a), the input current can be written as,

$$I_{in} = I_{A1} - I_{b1} \quad (2)$$

Where, I_{A1} is the input leakage current of the OPAMP A1, and I_{b1} is the back-gate current of the transistor *MP1*.

As shown in Fig. 1(a), *MP1* forms a voltage-controlled-capacitor, the gate voltage is the output voltage of the amplifier A1, and the source terminal is connected to the reference ground. The back-gate current (I_{b1}) of *MP1* is determined by the drain voltage (V_D). This drain voltage is generated by a voltage feedback loop, shown in Fig. 1(b).

As shown in Fig. 1(b), the voltages held at the source and gate terminal of *MP2* are the same as that of *MP1*. The back-gate voltage of *MP2* is connected to the terminal '-' of A2. The output of A2 provides that voltage (V_D) which is necessary to ensure the back-gate current of *MP2* (I_{b2}) delivers the leakage current for the terminal '-' of A2. The terminal '+' of *A2* is defined by V_f. The leakage currents into the input terminals of A1 and A2 are equal, due to circuit feedback and the terminal voltages being the same. The voltage V_D is also applied to the drain of *MP1* to yield the same amount of the back-gate current as *MP2*,

$$I_{b2} \approx I_{b1} \approx I_{A1} \quad (3)$$

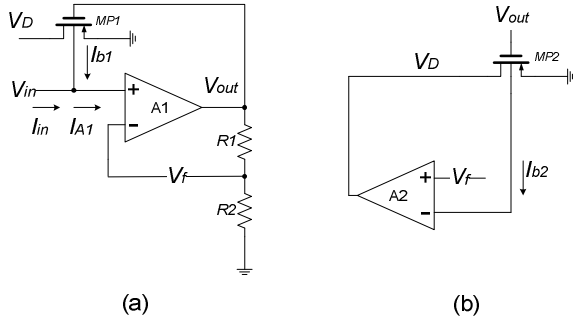

Fig. 1 *Circuit of (a) back-gate current neutralisation FEA. (b) Drain voltage generation circuit.*

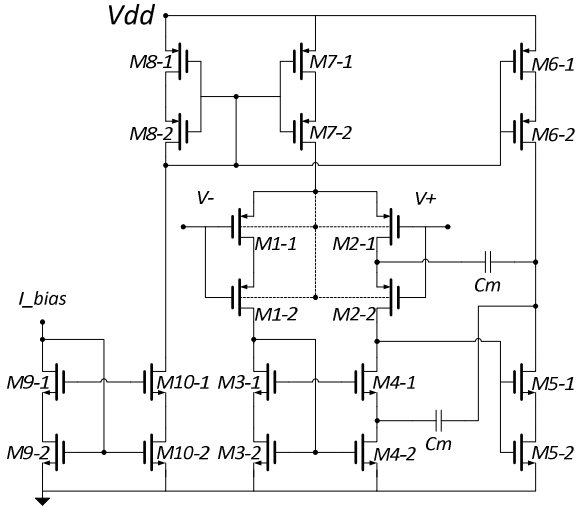

Fig. 2 *Circuit schematic of low noise two-stage CMOS OPAMP*

The AC currents at the input stage of the BCN are shown in Fig. 3, the input voltage is 1 V. The leakage current of the OPAMP A1, I_{A1}, increases with increasing frequency. The back-gate current, I_{b1}, neutralises the leakage current to minimise the input current, I_{in}. The input impedance of the OPAMP A1 is approximately 4.6 GΩ at 1 KHz. When the BCN neutralisation is implemented, the impedance of the FEA increases to circa 41.7 GΩ.

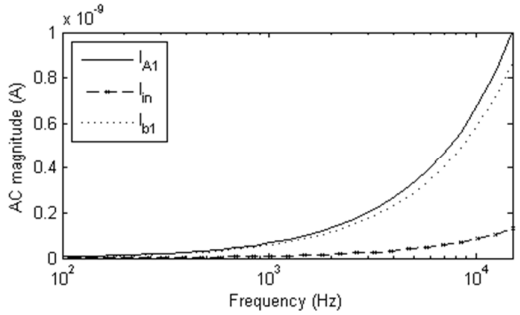

Fig. 3 *AC currents of BCN*

The statistical variance intrinsic to IC manufacturing and the conditions of operation, characterised by Process, Voltage and Temperature (PVT) variations. PVT corners simulation is a standard evaluation tool for IC manufacturing. The frequency of the PVT simulations is 1 kHz.

The charts in Fig. 4 show process-corner simulations for the neutralisation schemes. The nomenclature (F-S) corresponds to fast-slow mobility corners of electron and hole carries. Mobility corners are written in the sequence of NMOS/PMOS. The fixed-value feedback capacitor is selected under the typical process corner (centre of manufacturing range), to maximise the input impedance of FCN [3]. The leakage currents vary across process corners for the transistors, as shown in Fig. 4(a), (c), (e) and (g), while the neutralisation current remains fixed. This indicates that the conventional FCN cannot effectively suppress the input current across process variation. As shown in Fig. 4(b), (d), (f) and (h), the simulated results prove that the BCN will always substantially compensate the input leakage current over process variation.

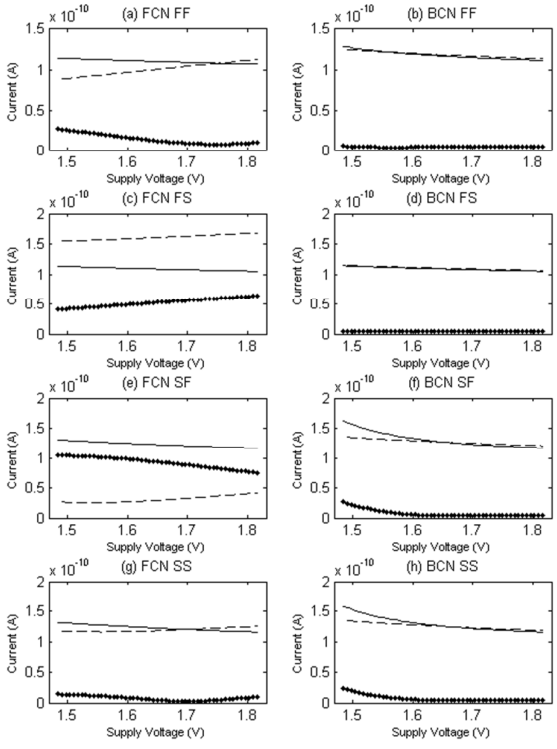

Fig. 4 *Process corners (a) FF of FCN. (b) FF of BCN. (c) FS of FCN. (d) FS of BCN. (e) SF of FCN. (f) SF of BCN. (g) SS of FCN. (h) SS of BCN.*

Performance, swept across voltage corners, is depicted in Fig. 5. A 10% voltage sweep is presented, 2.97 to 3.63 V for a nominal 3.3 V supply (compliant with industry practice). As shown in Fig. 5(a), the leakage current which dominated by the parasitic capacitance is sensitive to supply voltage variation. On the other hand, as given in Fig. 5(b), the BCN achieves a high input impedance across the standard supply voltage variations.

The temperature corner sweep is depicted in Fig. 6. The neutralisation current of the FCN, as shown in Fig. 6(a), reduces with increasing temperature, leadingto a decrease of the input impedance. The proposed BCN, as shown in Fig. 6(b), substantially minimises the difference between the leakage and neutralisation current. It achieves a constantly high input impedance across temperature variations.

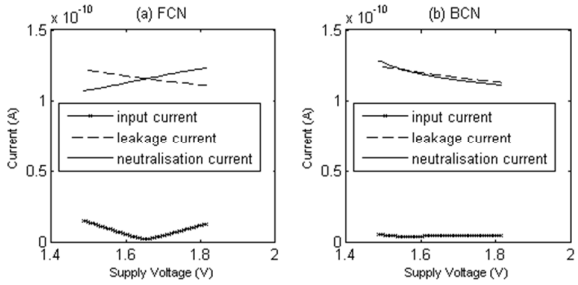

Fig. 5 *Voltage corner sweep of (a) FCN. (b) BCN.*

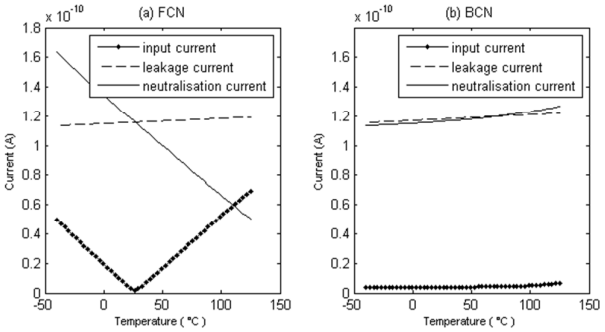

Fig. 6 *Temperature corner sweep of (a) FCN. (b) BCN.*

These results show that, the BCN technique compensates the input leakage current over all PVT corners.

Conclusion: In this paper, a new back-gate current neutralisation feedback technique for front-end neural applications is proposed. This FEA is targeted at IC implementation and is simulated on the AMS 0.35µm CMOS process [4]. It provides an input impedance of 41.7 GΩ (at 1 kHz) and consumes 22.1 µW in 0.078 mm^2. The FEA achieves a high input impedance by neutralising the gate leakage current using the BCN feedback loop, over a wide bandwidth and manufacturing and operational variations

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